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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,383	11/03/2003	Chan-kyung Kim	SEC.1052	2722

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,383	KIM, CHAN-KYUNG	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7 and 14-20* is/are rejected.

7)☒ Claim(s) *2-5 and 8-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 16, the limitation the first N-bit adder output signal from step (a1) recited on line 3 lacks antecedent basis. In other words, there is no step (a1) and there is no first N-bit adder output signal the recitation is referring to.

As per claim 17, the limitation the second N-bit adder output signal from step (b1) recited on line 10 lacks antecedent basis. In other words, there is no step (b1) and there is no second N-bit adder output signal the recitation is referring to.

As per claim 18, this claim is rejected because of the indefiniteness of claim 17.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 6-7, 14-15 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,570,425, issued to Yamaguchi.

As per claim 1, Yamaguchi discloses a delayed tap signal generating circuit (Fig. 8) comprising:

a first tap signal generating circuit (the combination of 802-1 and 803-1) adapted to receive a first clock signal (CLKIN1) and a second clock signal (CLKIN2), which have a same frequency and a phase difference between them (Figs. 9A and 9B), and adapted to generate a first tap signal (CK1) in response to the first and second clock signals and offset information (column 5, lines 29-32, the weighted information from the interpolators 802-1 and 802-2), wherein the first tap signal is delayed with respect to the first clock signal by a first delay (column 5, line 56, the first delay) corresponding to the offset information (column 5, line 56, shown is the relationship between CKIN1 and CK1); and

a second tap signal generating circuit (the combination of 802-2 and 803-2) adapted to receive the first and second clock signals (CKIN1 and CLKIN2), and adapted to generate a second tap signal (CK2) in response to the first and second clock signals and the offset information (the weighted information from the interpolators 802-1 and 802-2), wherein the second tap signal is delayed with respect to the first clock signal by the first delay and a second delay added to the first delay (column 6, line 3, shown is the relationship between CKIN1 and CK2 and the quantity of the delay),

wherein the first and second tap signals are generated by interpolating the first and second clock signals in response to the offset information (elements 802-1 and 802-2 are interpolators, column 5, lines 29-32).

As per claim 6, because the second delay is $\theta/3$ and the phase difference between the first and second clock signals is θ, the recited limitation is met.

As per claim 7, Yamaguchi discloses a delayed tap signal generating circuit (Fig. 10) adapted to receive a first clock signal (CKIN1) and a second clock signal (CLKIN2), which have

the same frequency and a phase difference between them (Figs. 9A and B), and adapted to generate a plurality of delayed tap signals (CKIN1, CK1, CK2), each of which has a delay less than the phase difference (compare between θ and θ/n), the circuit comprising:

a second tap signal generating circuit (1002-1 and 1003-1) adapted to generate a second tap signal (CK1) in response to the first and second clock signals and offset information, wherein the second tap signal is delayed with respect to a first tap signal by a first delay corresponding to the offset information (same as discussed in claim 1);

a third tap signal generating circuit (1002-2 and 1003-2) adapted to receive the first and second clock signals, and adapted to generate a third tap signal (CK2) in response to the first and second clock signals and the offset information, wherein third tap signal is delayed with respect to the first tap signal by the first delay and a second delay added to the first delay (same as discussed in claim 1); and

a fourth tap signal generating circuit (1002-3 and 1003-3) adapted to receive the first and second clock signals, and adapted to generate a fourth tap signal (CK3) in response to the first and second clock signals and the offset information, wherein the fourth tap signal is delayed with respect to the first tap signal by the first and second delays and a third delay added to the first and second delays (same as discussed in claim 1),

wherein the first tap signal is the first clock signal (as shown, it is CKIN1), and

wherein the second, third, and fourth tap signals (CK1, CK2 and CK3) are generated by interpolating the first and second clock signals in response to the offset information (1002-1, ..., 1002-n are interpolators).

As per claim 14, this claim is rejected for the same reason noted in claim 6.

As per claim 15, this is merely a method to operate a circuit having the structure discussed in claim 1, since Yamaguchi teaches the circuit, the method to operate is inherently taught.

As per claim 19, this claim is rejected for the same reason noted in claim 6.

As per claim 20, this is merely a method to operate a circuit having the structure discussed in claim 7, since Yamaguchi teaches the circuit, the method to operate is inherently taught.

Allowable Subject Matter

4, Claims 2-5 and 8-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-5 are allowable because the prior art of record fails to disclose or suggest the inclusion of a first N-bit adder and a first digital/analog converter in the first tap generating circuit as recited in claim 2.

Claims 8-13 are allowable for the same reason noted in claim 2.

5. Claims 16-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 16-18 are allowable for the same reason noted in claim 2.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/3/04

Minh Nguyen
Primary Examiner
Art Unit 2816